

REMARKS

The present application was filed on June 8, 2000 with claims 1-20. Claims 1-20 remain pending. Claims 1, 6, 13, and 20 are independent claims.

In the outstanding Office Action dated March 17, 2003, the Examiner: (i) rejected claims 2-20 under 35 U.S.C. §112, second paragraph, as being indefinite; (ii) rejected claims 1 and 2 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,646,332 to Suzuki (hereinafter "Suzuki"); (iii) rejected claims 1-5 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,905,667 to Lee (hereinafter "Lee"); (iv) rejected claims 6-9, 11, 13-16, 18 and 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,943,251 to Jiang et al. (hereinafter "Jiang"); (v) rejected claims 12 and 19 under 35 U.S.C. §103(a) as being obvious over Jiang in view of Lee; (vi) objected to the drawings under 37 C.F.R. §1.83(a); and (vii) objected to the disclosure due to informalities.

In response to the Office Action, Applicant amends claims 1, 2, 6, 7, 13, 14 and 20 for the reasons below.

Applicant acknowledges the indication of allowable subject matter in claims 10 and 17, but reserves the right to rewrite such dependent claims in independent form pending the disposition of the independent claims from which they depend.

With regard to the rejection of claims 2-20 under 35 U.S.C. §112, second paragraph, as being indefinite, Applicant asserts that such claims are patentable for at least the reasons that claims 2, 6, 7, 13, 14 and 20 from which claims 3-5, 8-12 and 15-19 directly or indirectly depend, are patentable. Claims 2, 6, 7, 13, 14 and 20 have been amended to more clearly set forth the invention in accordance with the suggestions offered in the Office Action. Accordingly, withdrawal of the rejection to claims 2-20 under 35 U.S.C. §112, second paragraph is therefore respectfully requested.

With regard to the rejection of claims 1 and 2 under 35 U.S.C. §102(b) as being anticipated by Suzuki, Applicant asserts that such claims are patentable for at least the reasons that independent claim 1, from which claim 2 directly depends, is patentable. Suzuki discloses a logical operation circuit device that includes a number of exclusive AND/OR logical elements derived from the logical formulas associated with a full adder/subtractor. The arrangement provides a full

adder/subtractor for operating on one-bit binary digital signals. Most importantly, Suzuki discloses static type logic circuits implemented by bipolar logic, static, or CPL.

Independent claim 1 of the present invention was amended to more clearly set forth the invention and discloses that the binary adder circuit has dynamic logic for generating the binary output value. Further, claim 1 provides that the binary output value is generated without one of a positive and a negative complementary version of the carry value. Support for this amendment can be found on page 3, lines 2-12 of the specification. Expressing the final sum bit in this form allows a simple implementation using a reduced number of dynamic logic gates. This provides the benefits of reduced power consumption and reduced circuit area due to the elimination of positive (or negative) complementary carry logic. Suzuki does not disclose dynamic circuits or the elements and benefits described above. Accordingly, withdrawal of the rejection to claims 1 and 2 under 35 U.S.C. §102(b) is therefore respectfully requested. X

With regard to the rejection of claims 1-5 under 35 U.S.C. §102(b) as being anticipated by Lee, Applicant asserts that such claims are patentable for at least the reasons that independent claim 1, from which claims 2-5 directly or indirectly depend, is patentable. Lee discloses an adder that includes a static logic block, a first dynamic inverter logic block, a dynamic logic block, and a second dynamic inverter logic block for generating a sum through a sum output node. Lee describes a dynamic logic version of an adder gate that uses a combination of inverting clock signals and short circuit current paths to conditionally discharge a dynamic node. This solution consumes excess power through the dc current path of the pullup device MN5 and MN71 in FIG. 5, with the pull-down trees. Lee also uses two clocks, CLK and inverted clock CLKB, to prevent a pre-discharge of the dynamic node NODE52. The outputs SUM and CARRY can be in a high-impedance floating state when CLK is low and neither the SUM or CARRY is evaluated and a HIGH signal. This creates a noise sensitivity problem. J 103 X

Independent claim 1 of the present invention has been amended to more clearly set forth the invention and disclose a binary adder circuit having dynamic logic without inversion of intermediate signals prior to a final stage. The present invention logically translates the signals so the only inversion of signal occurs at the final static output SUM stage illustrated in FIG. 4, and described 9 X

beginning on page 10, line 14 and extending to page 11, line 6 of the specification. All other signals driving dynamic nodes are non-inverting, avoiding the difficulties encountered in Lee and allowing the present invention to express the final sum in a simple implementation using a reduced number of dynamic logic gates. The elimination of a need for positive (or negative) complementary signal generation in the parallel adder allows for reduced power consumption and reduced circuit area. P-type pull-up trees are avoided since intermediate signals are not inverted prior to a final stage, thus also avoiding inherently slower p-type devices. These elements and their resulting benefits are not disclosed in Lee. Accordingly, withdrawal of the rejection to claims 1-5 under 35 U.S.C. §102(b) is therefore respectfully requested. X

With regard to the rejection of claims 6-9, 11, 13-16, 18 and 20 under 35 U.S.C. §102(e) as being anticipated by Jiang, Applicant asserts that such claims are patentable for at least the reasons that independent claims 6, 13 and 20, from which claims 7-9, 11, 14-16 and 18 directly or indirectly depend, are patentable. Jiang discloses an adder circuit having special carry blocking, propagating or generating cells filled with appropriate signals either by table look-up or circuit implementation using data type and processing type inputs. Jiang discloses static type logic circuits implemented by bipolar logic, static, or CPL

Independent claims 6, 13 and 20 were amended to more clearly set forth the invention and disclose a dynamic N-bit adder. Support for these amendments can be found on page 3, lines 2-12, X of the specification. The adder has a plurality of logic stages that generate a summation signal representing the logical addition of the first and second binary values generated without positive or negative complementary signal generation. The elimination of a need for positive (or negative) complementary signal generation in the parallel adder allows for reduced power consumption and reduced circuit area. Jiang does not disclose dynamic circuits or the elements and their resulting benefits described above. Accordingly, withdrawal of the rejection of claims 6-9, 11, 13-16, 18 and 20 under 35 U.S.C. §102(e) is therefore respectfully requested. Y

With regard to the rejection of claims 12 and 19 under 35 U.S.C. 103(a) as being obvious over Jiang in view of Lee, Applicant asserts that such claims are patentable for at least the reasons that independent claims 6 and 13, from which claims 12 and 19 directly depend, are patentable. The

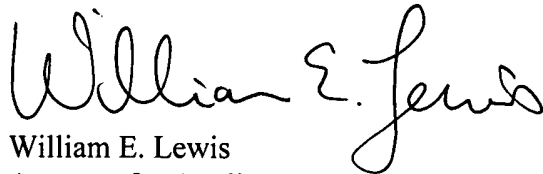
patentability of claims 6 and 13 are described above. Accordingly, withdrawal of the rejection of claims 12 and 19 under 35 U.S.C. 103(a) is therefore respectfully requested.

The drawings were objected to under 37 C.F.R. 1.83(a) for not showing every feature of the invention specified in the claims. Applicant asserts that all elements featured in the claims are shown in the drawings. The limitation of " $[p(n)*C(n-1)]*[p(n)+C(n-1)]$ " from claim 2, line 2, is defined as the output signal  $S(n)$ . This limitation is also defined as  $S(n)$  in equation (3), on page 3, line 5 of the present specification.  $S(n)$  is illustrated in FIG. 1. Accordingly, withdrawal of the objection to the drawings is therefore respectfully requested.

The abstract was amended to correct a minor error of a grammatical nature in accordance with the suggestion offered in the Office Action. Attached hereto is a marked-up version of the changes made to the specification and claims by the present Amendment.

In view of the above, Applicant believes that claims 1-20 are in condition for allowance, and respectfully request withdrawal of the §112, §102(b), §102(e) and §103(a) rejections.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph in the Abstract has been amended as follows:

A dynamic parallel adder is provided which eliminates the positive (or negative) complimentary carry generate and propagate signal logic normally used to implement a conventional dynamic parallel added. The method for implementing the incentive adder users a novel XOR configuration constructed with dynamic CMOS logic circuits.

[1500-44.APP]

IN THE CLAIMS

1. (Amended) Apparatus for use in summing at least two binary values, comprising:  
a binary adder circuit, responsive to a first binary value, a second binary value and a carry value, and operative to generate a binary output [value] signal S(n) representative of a summation of the first binary value, the second binary value and the carry value, the binary adder circuit having dynamic logic, without inversion of intermediate signals prior to a final stage, for implementing an exclusive OR function that generates the binary output value without one of a positive and a negative complementary version of the carry value.

2. (Amended) The apparatus of claim 1, wherein the binary output signal S(n) is [represented by] implemented in accordance with an expression:  $\wedge(p(n) * C(n-1)) * (p(n) + C(n-1))$ , where C(n-1) is a generate signal from a binary value n-1 associated with the carry value, p(n) is a propagate signal associated with the first binary value and the second binary value,  $\wedge$  is a logical complement operator, \* is an AND operator, and + is an OR operator.

6. (Amended) [An] A dynamic N-bit parallel adder, comprising:  
a first logic stage, the first logic stage configured to receive a first N-bit binary value and a

second  $N$ -bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through  $m$  bits from the generate and propagate signals computed in the first logic stage;

a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without [the] a need for one of positive and negative complementary signal generation.

7. (Amended) The parallel adder of claim 6, wherein a generate signal and a propagate signal computed for a bit  $i$  in the first logic stage represent a carry signal  $c_i$ , wherein  $c_i$  is equivalent to  $g_i + (p_i c_{i-1})$ , where  $g_i$  represents the generate signal and is equivalent to a logical multiplication operation between  $a_i$  and  $b_i$  where  $[a]$   $a_i$  represents the first binary value and  $[b]$   $b_i$  represents the second binary value, and where  $p_i$  represents the propagate signal and is equivalent to a logical summation operation between  $a_i$  and  $b_i$ .

13. (Amended) A method of adding, in parallel, a first  $N$ -bit binary value and a second  $N$ -bit binary value, the method comprising the steps of:

computing generate signals and propagate signals for each bit;

computing block generate signals and block propagate signals for groups of one through  $m$  bits from the generate and propagate signals computed in the first computing step;

combining the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

combining remaining uncombined block generate and block propagate signals with a

propagate signal associated with each bit, and generating a summation signal wherein the summation signal represents the dynamic logical addition of the first and second binary values and the summation signal is generated without a [the] need for one of positive and negative complementary signal generation.

14. (Amended) The method of claim 13, wherein a generate signal and a propagate signal computed for a bit  $i$  in the first logic stage represent a carry signal  $c_i$ , wherein  $c_i$  is equivalent to  $g_i + (p_i c_{i-1})$ , where  $g_i$  represents the generate signal and is equivalent to a logical multiplication operation between  $a_i$  and  $b_i$  where  $[a]$   $a_i$  represents the first binary value and  $[b]$   $b_i$  represents the second binary value, and where  $p_i$  represents the propagate signal and is equivalent to a logical summation operation between  $a_i$  and  $b_i$ .

20. (Amended) A processing device having [an] a dynamic  $N$ -bit parallel adder, the dynamic  $N$ -bit parallel adder comprising:

a first logic stage, the first logic stage configured to receive a first  $N$ -bit binary value and a second  $N$ -bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through  $m$  bits from the generate and propagate signals computed in the first logic stage;

a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without [the] a need for one of positive and negative complementary signal generation.